PENDING CLAIMS

The following is a complete list of currently pending claims. Please cancel claims 1-19, 35-44, and 50-70. Claims 20 and 45 are amended as shown below.

1.-19. (Cancelled)

20. (Currently amended) ~~The array of claim 19~~, A nonvolatile memory array, comprising:

an array of nonvolatile memory devices;

at least one driver circuit; and

a substrate;

wherein the at least one driver circuit is not located in a bulk monocrystalline silicon substrate, wherein the array of nonvolatile memory devices comprises an array of PROMs, EPROMs or EEPROMs, wherein the array of nonvolatile memory devices comprises a monolithic three dimensional array of memory devices.

21. (Withdrawn) The array of claim 20, wherein the array of nonvolatile memory devices comprises a three dimensional array of antifuses.

22. (Withdrawn) The array of claim 21, wherein the array of antifuses comprise a first set of rail stack conductors, a second set of rail stack conductors extending in a different direction than the first set of rail stack conductors, and an insulating layer disposed between the first and the second sets of rail stacks.

23. (Withdrawn) The array of claim 22, further comprising semiconductor diodes located at intersections of the conductors of the first and the second sets of rail stacks.

24. (Withdrawn) The array of claim 23, wherein the diodes comprise P+ / N- diodes.

25. (Previously amended) A nonvolatile memory array, comprising:

an array of nonvolatile memory devices;

at least one driver circuit; and

a substrate;

wherein the at least one driver circuit is not located in a bulk monocrystalline silicon substrate, wherein the array of nonvolatile memory devices comprises an array of PROMs, EPROMs or EEPROMs, wherein the array comprises:

a first plurality of spaced-apart conductors disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed above the first height in a second direction different from the first direction, each rail-stack including a semiconductor film of a first conductivity type in contact with said first plurality of spaced-apart conductors, a local charge storage film disposed above the semiconductor film and a conductive film disposed above the local charge storage film.

26. (Original) The array of claim 25, wherein:

a space between said spaced-apart conductors contains a planarized deposited oxide material;

said semiconductor film comprises polysilicon; and

said local charge storage film is selected from a group consisting of a dielectric isolated floating gate, an ONO dielectric film and an insulating layer containing conductive nanocrystals.

27. (Withdrawn) The array of claim 20, wherein each device of the three dimensional array comprises:

a first conductor;

a second conductor; and

a pillar vertically disposed between the first and the second conductors;

wherein the pillar comprises:

a semiconductor diode having a first conductivity type region and a second conductivity type region;

a tunneling oxide;

a charge storage region; and

a blocking oxide.

28. (Withdrawn) The array of claim 20, wherein each memory device of the three dimensional array comprises:

a source region, a channel region and a drain region each vertically aligned with one another to form a pillar;

a first electrode contacting the source region;

a second electrode contacting the drain regions;

a charge storage region located adjacent to and in contact with the channel region; and

a control gate located adjacent to and in direct contact with the charge storage region.

29. (Withdrawn) The array of claim 20, wherein the array of nonvolatile memory devices comprises an array of TFT EEPROMs.

30. (Withdrawn) The array of claim 29, wherein the array comprises:

a plurality of vertically separated device levels, each level comprising an array of TFT EEPROMs, each TFT EEPROM comprising a channel, source and drain regions, a control gate, and a charge storage region between the channel and the control gate;

a plurality of bit line columns in each device level, each bit line contacting the source or the drain regions of the TFT EEPROMs;

a plurality of word line rows in each device level; and

at least one interlayer insulating layer located between the device levels.

31. (Withdrawn) The array of claim 30, wherein:

the channel of each TFT EEPROM comprises amorphous silicon or polysilicon;

the columns of bit lines extend substantially perpendicular to a source-channel-drain direction of the TFT EEPROMs;

each word line contacts the control gates of the TFT EEPROMs, and the rows of word lines extend substantially parallel to the source-channel-drain direction of the TFT EEPROMs; and

the word lines are self aligned to the control gates of the array of TFT EEPROMs and the word lines are self aligned to the channel and the charge storage regions of the TFT EEPROMs located below the respective word lines.

32. (Withdrawn) The array of claim 27, wherein each charge storage region comprises:

an ONO dielectric film;

an insulating layer containing conductive nanocrystals; or

an isolated floating gate comprising:

a tunnel dielectric above the channel;

the floating gate above the tunnel dielectric; and

a control gate dielectric above the floating gate.

33. (Withdrawn) The array of claim 20, wherein the array of nonvolatile memory devices comprises a flash memory array which is programmed by FN tunneling.

34. (Withdrawn) The array of claim 33, wherein the array comprises:

a first plurality of spaced-apart conductive bit lines disposed at a first height above the substrate in a first direction; and

a second plurality of spaced-apart rail-stacks disposed at a second height in a second direction different from the first direction, each rail-stack including a plurality of semiconductor islands whose first surface is in contact with said first plurality of spaced-apart conductive bit lines, a conductive word line, and charge storage

regions disposed between a second surface of the semiconductor islands and the word line.

35-44. (Cancelled)

45. (Withdrawn; currently amended) ~~The array of claim 41,~~ A nonvolatile memory array, comprising:

a monocrystalline silicon substrate;

at least one driver circuit formed above the substrate; and

an array of nonvolatile memory devices formed above the substrate,

wherein the array of nonvolatile memory devices comprises a monolithic three dimensional array of memory devices.

46. (Withdrawn) The array of claim 45, wherein the array of nonvolatile memory devices comprises a three dimensional array of antifuses.

47. (Withdrawn) The array of claim 46, wherein the array of antifuses comprise a first set of rail stack conductors, a second set of rail stack conductors extending in a different direction than the first set of rail stack conductors, and an insulating layer disposed between the first and the second sets of rail stacks.

48. (Withdrawn) The array of claim 47, further comprising semiconductor diodes located at intersections of the conductors of the first and the second sets of rail stacks.

49. (Withdrawn) The array of claim 48, wherein the diodes comprise P+ / N- diodes.

50.-70. (Cancelled)